Performance of 1–10-GHz Traveling Wave Amplifiers in 0.18-μm CMOS

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***Abstract*—This letter presents two four-stage traveling-wave amplifiers (TWA) fabricated in a 0.18-μm CMOS process. A TWA with an internal drain bias network achieved a gain of 5 dB out to 10 GHz, and another TWA without an on-chip bias network achieved a gain of 8 dB out to 10 GHz. These are the highest frequency CMOS TWAs known to the authors.**

***Index Terms*—CMOS, microwave circuits, MOSFETs, traveling wave amplifiers.**

I. Introduction

TRAVELING wave amplifiers (TWA) have been a common topology for realizing broadband amplifiers in traditional microwave technologies, but it is relatively recently that they have been implemented in CMOS processes. Since CMOS is a very cheap technology, using it to fabricate high speed circuits may result in significant cost reductions.

In [1], a TWA was presented in a 0.8-μm CMOS process that used packaging inductance and bond-wires for the inductive elements. It achieved 5 ± 1.2-dB gain from 300 kHz to 3 GHz. In [2], a three stage TWA in a 0.18-μm CMOS process was presented that demonstrated a low frequency gain of 5 dB, sloping down to 1 dB at 15 GHz.

In [3], the first practical distributed amplifier (DA) in a standard digital CMOS process was presented. It was a four-stage DA using 0.6-μm MOSFETs and spirals inductors, achieving 6.5 ± 1.2 dB from 0.5 to 4 GHz.

This letter presents two four-stage TWAs designed in a 0.18-μm CMOS process with high impedance coplanar waveguides as the inductive elements. One TWA requires external biasing, and exhibits the highest gain of any CMOS TWA that operates out to 10 GHz known to the authors. The other uses a cascade of pMOSFETs as an internal drain bias network, and is the first CMOS TWA known to the authors that uses an internal bias network on the drain line. This eliminates the need for an off-chip bias network.

Fig. 1 shows the TWA with the on-chip drain bias network. The other version looks similar except with no bias network at the top.

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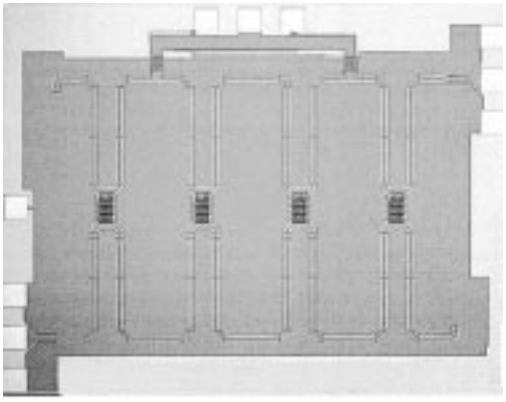

Fig. 1. Picture of TWA with drain bias network.

II. Challenges in Design of CMOS TWA

The use of silicon as a substrate for a TWA presents some particular design challenges over those posed to designers using standard microwave technologies. These include high input resistance at the gate, low output impedance at the drain, low transconductance, and lossy low impedance transmission lines. Most TWAs use single transistors or cascodes as gain blocks, which is suitable for HBT and MESFET designs. However, since the silicon MOSFET is inferior at high frequencies another topology was chosen for these circuits.

Fig. 2 shows the topology used for the gain blocks in the TWA. It is a combination of a Darlington connection, and a cascoded connection.

This topology offers several advantages over a single FET. First, the input capacitance is roughly the series combination of the $C_{\rm gs}$ of M_1 and M_3, which is less than that of a single FET of similar dimensions. The input resistance is reduced by using multiple-fingered narrow, double connected gates for M_1 and the input capacitance by using fewer gate fingers than the other transistors. M_3 may be made wider to improve the gain of the structure. M_2 is simply a biasing device, and is often replaced by a resistor in the Darlington configuration. The output resistance, which is quite low for a Darlington, is improved by the addition of M_4.

The measured input and output impedances of the Darlington cascodes are shown in Fig. 3. The input resistance [$\Re(S_{11})$] is much lower than is possible with a single FET without compromising gain. The input and output capacitances in the model used for design were approximately 220 fF.

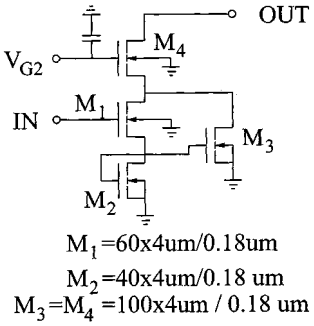

Fig. 2. Darlington cascode configuration used for each gain cell.

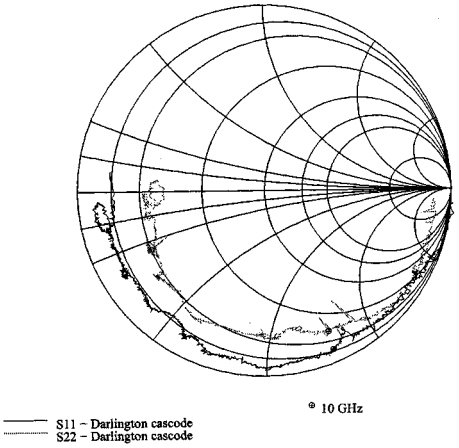

Fig. 3. Measured S_{11} and S_{22} of Darlington cascode from 0.04 to 40 GHz.

III. TWA With Drain Bias Network

Previous CMOS TWAs have used external biasing networks at the drains. This, however, leads to extremely large dc currents flowing at the output of the device that significantly exceed the recommended current density for the process. The transmission line widths must be relatively narrow to provide the necessary characteristic impedance, and to keep the RF losses low.

Fig. 4 shows the schematic of a TWA designed with internal bias networks. These reduce the maximum current density on the transmission lines by a factor of four and eliminate the need for off-chip biasing. They do, however, add additional capacitance and losses to the drain line which reduces its cutoff frequency and gain. This could easily be implemented as a current mirror, but for this circuit was not in order to allow additional freedom in testing. The two pMOS devices were designed to provide a large input resistance looking into the drain. However, the measured results show that the input resistance of the bias network reduces the gain of the internally biased TWA compared to the external version.

IV. Design and Fabrication

The TWAs were designed using S-parameter measurements from the 0.18-μm nonepitaxial process, and are approximately 1800×1300 μm. The substrate conductivity is approximately 10 S/m. 1-μm-thick aluminum on the top metal layer was used for all transmission lines, which are coplanar waveguides (CPW) [4]. The CPW gate and drain lines are all approximately

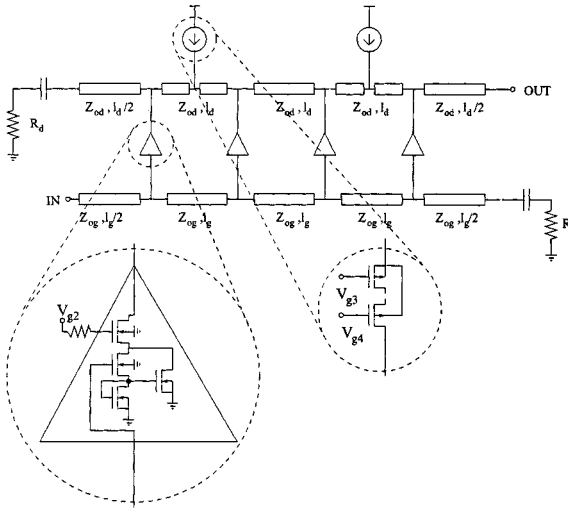

Fig. 4. Schematic of traveling wave amplifier with internal drain bias networks.

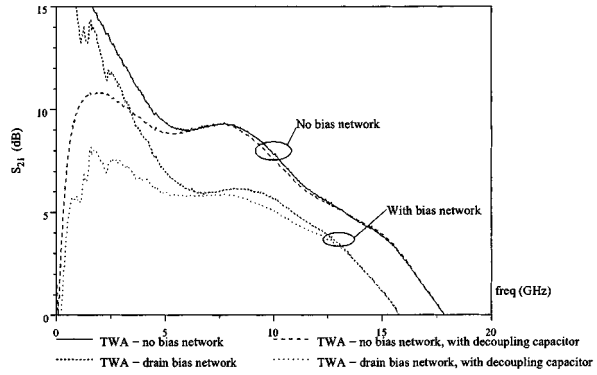

Fig. 5. Measured gain of TWAs.

70 Ω, and have a center thickness of approximately 10 μm. Versions of the TWA with and without the drain bias network were designed; other than the bias network itself the only differences between the two designs are the length of the gate and drain transmission lines between cells (the lines are approximately 1000 μm long for the internally biased version and 900 μm for the other). In the internal bias version, these lines were lengthened to take into account the additional capacitance due to the bias networks.

Fig. 5 shows the measured gain of two versions of the TWA. One has an internal bias network at the drain consisting of a cascade of pMOSFETs. This is the first CMOS TWA with a drain bias network known to the authors. The second has no drain bias network. The gain difference between the noninternally biased and biased versions is 3 dB due to additional absorption in the bias network. The increased low frequency gain is due to the *RC* terminating network in the gate and drain lines. Without the capacitors in the terminating networks the low frequency gain is much flatter, but the efficiency of the TWA is reduced due to additional current flow into the terminating resistors.

For measurement simplicity, no decoupling capacitor was included at the input of the TWA. With this capacitor added in simulation, the gain of the TWA without the drain bias network remains within ± 1 dB of the nominal gain between 1 and 10 GHz.

The ripple of the TWA with the drain bias network is more severe. These ripples are thought to be due to the fact the the design was based on measured transistor S-parameters which have been found to vary significantly between fabrication runs. The design of CMOS devices at 10 GHz is made difficult by the lack of good quality transistor models from fabrication facilities at microwave frequencies. Further optimization using superior models should improve this ripple.

V. Conclusion

Two TWAs have been presented which operate between 1 and 10 GHz. One version uses an internal bias network, the first known CMOS TWA to use an internal bias network, and provides 5-dB gain out to 10 GHz. The significant ripple in the gain through the passband is thought to be due to the transistor model used. The gain difference between the noninternally biased and biased versions is 3 dB due to additional absorption in the bias network.

Acknowledgment

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References

[1] P. Sullivan, B. Xavier, and W. Ku, "An integrated CMOS distributed amplifier using packaging inductance," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 1969–1975, Oct. 1997.

[2] B. Kleveland, C. Diaz, D. Vook, L. Madden, T. Lee, and S. Wong, "Monolithic CMOS distributed amplifier and oscillator," in *IEEE Int. Solid-State Circuits Conf. Dig.*, 1999, pp. 70–71.

[3] B. Ballweber, R. Gupta, and D. Allstot, "A fully integrated 0.5–5.5 GHz CMOS distributed amplifier," *IEEE J. Solid-State Circuits*, vol. 35, pp. 231–239, Feb. 2000.

[4] M. Riaziat, R. Majidi-Ahy, and I. Feng, "Propagation modes and dispersion characteristics of coplanar waveguides," *IEEE Trans. Microwave Theory Tech.*, vol. 38, pp. 245–251, Mar. 1990.